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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,763	05/11/2001	Heinrich Meyer	71-01	7120

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EXAMINER
MUTSCHLER, BRIAN L

ART UNIT	PAPER NUMBER
1753	

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6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/831,763	MEYER ET AL.
	Examiner	Art Unit
	Brian L. Mutschler	1753

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 May 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

   a. On page 5 at the fourth line in section (f), please change "Damaszene" to --Damascene--.

   b. On page 6 in the second full paragraph, please remove the reference to claim 1. Since the claims can change throughout the prosecution of the application, the reference is indefinite and should not be used.

   c. On page 19 at the first line in the third full paragraph, please change, "Damaszene" to --Damascene--.

   d. The specification should include a brief description of the drawings.

   Appropriate correction is required.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)),

and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)

(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(f) BRIEF SUMMARY OF THE INVENTION.

(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(h) DETAILED DESCRIPTION OF THE INVENTION.

(i) CLAIM OR CLAIMS (commencing on a separate sheet).

(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

2. Claim 1 is objected to because of the following informalities:

a. In claim 1 at line 3, please change "producting" to --producing--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "more especially in recesses having a high aspect ratio" in lines 3-4. This limitation is indefinite because it is not clear whether the recesses actually have high aspect ratios, or if the method applies to all recesses. For the purpose of examination, the broadest interpretation of the limitation was used, i.e., the method is for any recess. The same applies to dependent claims 2-9.

Claim 1 recites the limitation "at least one additive compound for controlling the physico-mechanical properties of the copper layers as well as Fe(II) compounds and/or Fe(III) compounds" in lines 14-17. This limitation is indefinite because it appears that the additive compound is controlling the properties of an iron compound, as opposed to the copper deposition bath containing Fe(II) compounds and/or Fe(III) compounds. Since the specification defines the bath as containing iron compounds, it was assumed that the additive compound only controls the properties of the copper layers and the copper deposition bath includes the iron compounds. It is suggested that the language in the claim be amended to clarify the limitations. The same applies to dependent claims 2-9.

Claim 1 recites the limitation "the semiconductor substrates" in lines 18-19. There is insufficient antecedent basis for this limitation in the claim. First, the prior limitations recited "semiconductor substrate surfaces", not a semiconductor substrate. Second, only one substrate was introduced, as opposed to a plurality of substrates implied by the term "substrates". The same phrase also occurs in line 22. It is suggested that the limitation be changed to --the semiconductor substrate surfaces--. The same applies to dependent claims 2-9.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2 and 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over DE 195 45 231 A1, herein referred to as DE '231, an optionally in view of Landau (U.S. Pat. No. 6,261,433). The rejection set forth below uses column and line number references provided by the English language version of DE '231, U.S. Pat. No. 6,099,711, which claims priority from DE '231 and therefore discloses the same invention.

DE '231 discloses a method for electroplating copper on circuit boards comprising the following steps:

a) Coating the surface of the substrate with a full-surface metal layer. In Example 1, DE '231 uses a circuit board having recesses (borings) in its surface that is provided with a thin copper laminate on the surfaces and a thin copper layer in the recesses, i.e., a substrate surface that has been coated (col. 12, lines 8-15).

b) Full surface deposition of copper layers having a uniform layer thickness by an electrolytic metal deposition method. In Example 4, a uniform layer of copper was electroplated on the copper foil covering the circuit board

(col. 13, lines 16-21). The copper was deposited using a bath, wherein the deposition step comprised:

i. A copper ion source, additives to improve the physical-mechanical properties, and a Fe(II) compound (col. 11, line 56 to col. 12, lines 6).

ii. An electric voltage was applied between the substrate and a dimensionally stable, insoluble counter-electrode (col. 13, lines 1-3 and lines 17-19).

The process of electroplating the copper layer and the buildup of the copper layer "structures" the copper layer.

Regarding claim 2, the current can be changed with a sequence of unipolar or bipolar pulses per unit time (figs. 1 and 2; col. 5, line 30 to col. 6, line 5).

Regarding claims 4 and 5, the anodic current pulse is set to at least the current of the cathodic current pulses and is preferably two to three times as high as the value of the cathodic current pulses (col. 5, lines 46-50).

Regarding claim 6, the additive compound disclosed by DE '231 can include polymeric oxygen-containing compounds (e.g., polyethylene glycol), organic sulphur compounds, thiourea compounds and polymeric phenazonium compounds (col. 8, line 26 to col. 2, line 21).

Regarding claims 7 and 8, the counter-electrode may comprise expanded titanium metal coated with iridium oxide, irradiated with fine particles (col. 16, lines 3-5).

Regarding claim 9, iron compounds are used to maintain the concentration of copper ions in the system by dissolution of copper pieces (col. 14, lines 46-67 and col. 16, lines 6-16).

The method of DE '231 differs from the instant invention because DE '231 does not disclose that the substrate can be a semiconductor substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a semiconductor substrate in place of the circuit board substrate disclosed by DE '231 because semiconductor substrates and circuit board substrates have equivalent properties and one skilled in the art would recognize that the method would be capable of forming a copper layer on either type of substrate. Both semiconductor substrates and circuit board substrates are dielectric materials requiring a conductive layer, or seed layer, on which to plate. Since the actual method of electroplating occurs on the seed layer, one skilled in the art would recognize that the actual "substrate" is irrelevant, i.e., the "substrate" can be any material, because the effective substrate on which the copper layer is plated is the conductive seed layer. Additionally, the prior art has recognized that electroplating on semiconductors is equivalent to electroplating on semiconductors. For example, Landau teaches, "As a result of these process limitations [i.e., the unsatisfactory results of CVD] electroplating, which had previously been limited to the fabrication of patterns on circuit boards, is just now emerging as a method to fill vias and contacts on semiconductor devices" (col. 2, lines 7-19).

7. Claims 1, 2 and 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ritzdorf et al. (US 2002/0074233 A1) in view of either Schumacher et al. (U.S. Pat. No. 5,976,341) or DE 43 44 387 A1, herein referred to as DE '387. Since the patent issued to Schumacher et al. claims priority to DE '387, and therefore both references disclose the same invention, the column and line number references made below will be made with respect to the English language document.

Ritzdorf et al. disclose a method for electroplating a semiconductor wafer comprising recessed structures, wherein the method comprises the following steps:

a) Coating the semiconductor substrate surfaces with a base layer. The substrate **400** is coated with a barrier layer **423** and a seed layer **425** (fig. 2D; page 3, par. [0036]-[0037]).

b) Full surface deposition of a copper layer having a uniform layer thickness on the base layer. A uniform layer of copper **440** is deposited on the seed layer **425** by an electrochemical deposition process (fig. 2E; par. [0038]-[0039]). The electroplating step comprises:

   i. A copper deposition bath containing a copper ion source and an additive (par. [0044]).

   ii. An electric voltage is applied between the semiconductor substrate and an inert anode, which would be dimensionally stable and insoluble in the deposition bath (par. [0031] and [0047]).

c) Structuring the copper layer. In addition to building up the copper layer **440**, excess materially is subsequently removed (fig. 2F; par. [0039]).

Regarding claim 2, the current may be a forward pulsed current or a forward and reverse current (par. [0047]).

Regarding claim 6, the additive may comprise polyethylene glycol, a polymeric oxygen-containing compound (par. [0044]).

The method of Ritzdorf et al. differs from the instant invention because Ritzdorf et al. do not disclose the following:

a. An Fe(II) compound or Fe(III) compound in the copper deposition bath, as recited in claim 1.

b. Inert metals coated with noble metals or oxides of the noble metals are used as the counter-electrode, as recited in claim 7.

c. Expanded titanium metal coated with iridium oxide and irradiated by means of fine particles is used as the counter-electrode, as recited in claim 8.

d. The concentration of the compounds of the copper ion source in the copper deposition bath is kept constant per unit time by contacting copper parts that are dissolved by reacting with Fe(III) contained in the bath, as recited in claim 9.

Regarding claims 1 and 9, Schumacher et al. disclose a method of electrochemically depositing copper on a circuit board substrate and teach the use of Fe(II) compounds and Fe(III) compounds in the deposition bath to generate copper ions and maintain the copper ion concentration (col. 6, lines 37-40; col. 8, lines 37-49).

Because inert anodes are used, iron compounds are provided to generate copper ions using copper parts (col. 8, lines 12-49).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of Ritzdorf et al. to use iron compounds and copper parts to generate copper ions as taught by Schumacher et al. and DE '387 because the iron compounds and copper parts provide the copper necessary for plating copper when inert anodes are used.

Regarding claims 7 and 8, like Ritzdorf et al., Schumacher et al. disclose the use of insoluble counter-electrodes when electroplating copper (col. 8, lines 12-36). Schumacher et al. further teach that titanium anodes with an iridium oxide coating surface treated to be compacted are sufficiently resistant and have a long lifespan (col. 8, lines 17-20). Expanded metal may also be used to increase the effective surface (col. 8, lines 33-36).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the inert counter-electrode in the method of Ritzdorf et al. to use an expanded titanium metal counter-electrode coated with iridium oxide as taught by Schumacher et al. and DE '387 because such an electrode is sufficiently resistant and has a long lifespan for electroplating copper.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ritzdorf et al. (US 2002/0074233 A1) in view of either Schumacher et al. (U.S. Pat. No.

5,976,341) or DE 43 44 387 A1, as applied above to claims 1, 2 and 6-9, and further in view of Loch (U.S. Pat. No. 4,666,567).

Ritzdorf et al., Schumacher et al. and DE '387 describe a method having all of the limitations recited in claims 1, 2 and 6-9 of the instant application, as explained above in section 7.

The method described by Ritzdorf et al., Schumacher et al. and DE '387 differs from the instant invention because they do not disclose the following:

a. The sequence of bipolar pulses comprises cathodic pulses lasting from 20 milliseconds to 100 milliseconds and anodic pulses lasting from 0.3 milliseconds to 10 milliseconds, as recited in claim 3.

Loch discloses a method for electroplating using bipolar pulsed current, wherein the duration of the cathodic (forward) pulses ranges from about 0.5 microseconds to about 300 seconds and the anodic (reverse) pulses last from about 0.5 microseconds to about 150 seconds (col. 3, lines 40-45). Furthermore, Loch teaches a specific example comprising a forward pulse of about 30 milliseconds followed by a reverse pulse of about 0.5 milliseconds (col. 7, lines 64-67).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method described by Ritzdorf et al., Schumacher et al. and DE '387, to have used pulses lasting within the claimed ranges because Loch teaches that a wide range of pulse lengths can effectively be used and specifically teaches the use of pulse lengths within the claimed range that is efficient for plating.

9. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ritzdorf et al. (US 2002/0074233 A1) in view of either Schumacher et al. (U.S. Pat. No. 5,976,341) or DE 43 44 387 A1, as applied above to claims 1, 2 and 6-9, and further in view of GB 2 214 520 A, herein referred to as GB '520.

Ritzdorf et al., Schumacher et al. and DE '387 describe a method having all of the limitations recited in claims 1, 2 and 6-9 of the instant application, as explained above in section 7.

The method described by Ritzdorf et al., Schumacher et al. and DE '387 differs from the instant invention because they do not disclose the following:

a. The peak current of the anodic pulses is at least the same value as the peak current of the cathodic pulses, as recited in claim 4.

b. The peak current of the anodic pulses is two to three times greater than the peak current of the cathodic pulses, as recited in claim 5.

GB '520 discloses a method for electroplating using bipolar current pulses wherein the anodic pulses have the same or greater value as the peak cathodic current pulses (fig. 1 and 4; page 1, third full paragraph; page 5, second full paragraph). GB '520 teaches that a forward current of 3 amps/Dm and a reverse current of 5 amps/Dm are effective for plating a uniform thickness in holes on a circuit panel (see example results on page 9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method described by Ritzdorf et al.,

Schumacher et al. and DE '387 to use a higher current (two to three times higher) in the anodic pulses than the cathodic pulses as taught by GB '520 because using a higher anodic current than cathodic current has been shown to deposit a more uniform copper layer in recesses.

Double Patenting

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 1, 2 and 4-9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of U.S. Patent No. 6,099,711 in view of DE 195 45 231 A1 and optionally in view of Landau (U.S. Pat. No. 6,261,433).

US '711 claims a method for the electrolytic deposition of metal coatings including the deposition of copper on surfaces and bores of circuit boards (claim 10) comprising the steps of:

a) Applying a pulse current, including both anodic and cathodic pulses, to a workpiece polarized as a cathode (claim 1).

b) Using inert, dimensionally stable, insoluble anodes (claim 1).

c) Using a deposition bath comprising ions of the metal to be plated (claim 1), additive compounds for controlling fracture elongation (claim 1) and compounds of a reversible redox system including Fe(II) and Fe(III) compounds (claims 1 and 8).

The process of electroplating the copper layer and the buildup of the copper layer "structures" the copper layer.

Regarding claims 2, 4 and 5, US '711 claims that anodic and cathodic pulses are used and that the anodic pulse current is two to three times greater than the cathodic pulse current (claim 3).

Regarding claims 7 and 8, US '711 claims that titanium expanded metal layered with iridium oxide irradiated with fine particles is used as an anode (claim 7).

Regarding claim 9, pieces of the metal (i.e., copper in the case of claim 10) are dissolved by the iron compounds, which would generate metal ions in the deposition bath (claim 1).

The method of US '711 differs from the instant invention because US '711 does not disclose the following:

a. The substrate is a semiconductor substrate surface, as recited in claim 1.

b. Coating the semiconductor substrate surfaces with a base (basic) metal layer, as recited in claim 1.

c. The additive comprises polymeric oxygen-containing compounds, organic sulphur compounds, thiourea compounds and polymeric phenazonium compounds, as recited in claim 6.

Regarding claim 1, in Example 1, DE '231 uses a circuit board having recesses (borings) in its surface that is provided with a thin copper laminate on the surfaces and a thin copper layer in the recesses, i.e., a substrate surface that has been coated (col. 12, lines 8-15).

Since most circuit boards are made of dielectric materials, i.e., they must be modified before they can be electroplated upon, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the method of US '711 to coat the substrate with a metal layer as taught by DE '231 because coating with a metal layer would allow copper to be electroplated on the circuit board substrate. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a semiconductor substrate in place of the circuit board substrate claimed by US '711 because semiconductor substrates and circuit board substrates have equivalent properties and one skilled in the art would recognize that the method would be capable of forming a copper layer on either type of substrate. Both semiconductor substrates and circuit board substrates are dielectric materials requiring a conductive layer, or seed layer, on which to plate. Since the actual method of electroplating occurs on the seed layer, one skilled in the art would recognize that the actual "substrate" is irrelevant, i.e., the "substrate" can be any material, because the effective substrate on which the copper layer is plated is the conductive seed layer.

Additionally, the prior art has recognized that electroplating on semiconductors is equivalent to electroplating on semiconductors. For example, Landau teaches, "As a result of these process limitations [i.e., the unsatisfactory results of CVD] electroplating, which had previously been limited to the fabrication of patterns on circuit boards, is just now emerging as a method to fill vias and contacts on semiconductor devices" (col. 2, lines 7-19).

Regarding claim 6, the additive compound disclosed by DE '231 can include polymeric oxygen-containing compounds (e.g., polyethylene glycol), organic sulphur compounds, thiourea compounds and polymeric phenazonium compounds (col. 8, line 26 to col. 2, line 21).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the additive in the method claimed by US '711 to use an additive including polymeric oxygen-containing compounds, organic sulphur compounds, thiourea compounds and polymeric phenazonium compounds as taught by DE '231 because such additives improve the fracture elongation and tensile strength of deposited copper.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Mutschler whose telephone number is (703)

305-0180. The examiner can normally be reached on Monday-Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (703) 308-3322. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9310 for regular communications and (703) 872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0661.

blm
June 12, 2003

NAM NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700